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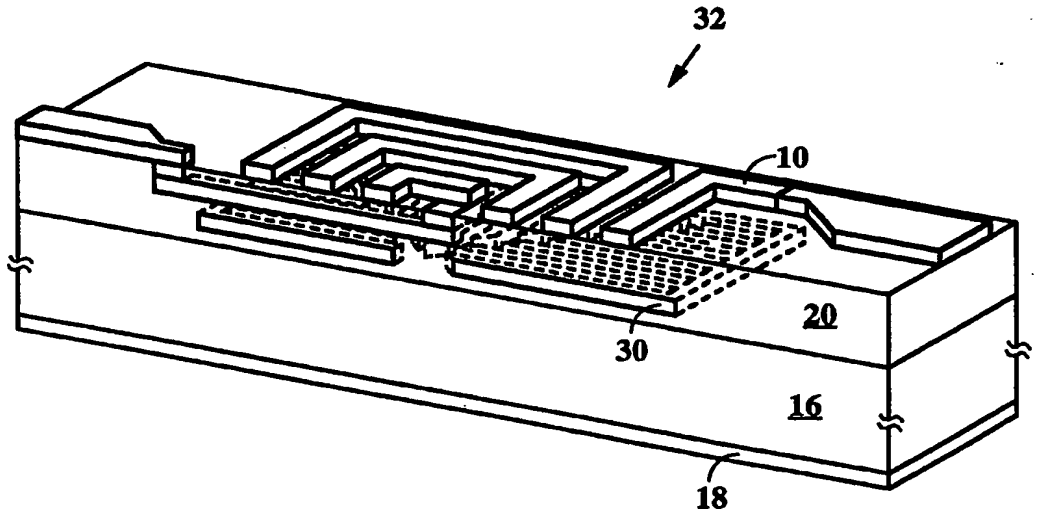

(57) Abstract

The performance of an integrated circuit spiral inductor is improved by fabricating a patterned ground shield [30] between the inductor [10] and the substrate [16]. The ground shield contains locally isolated conductive lines positioned substantially orthogonal to the conductive lines in the inductor, forming a grating that shields the inductor from the substrate without reducing the inductance of the inductor at high frequencies. The ground shield may also be positioned above an inductor to provide electrical shielding from other circuit elements fabricated above.

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PATTERNED GROUND SHIELDS FOR INTEGRATED CIRCUIT INDUCTORS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional Application 60/045,416 filed 05/02/97, which is incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates generally to integrated circuit technologies. More particularly, it relates to integrated circuits having high quality inductors with ground shields.

BACKGROUND OF THE INVENTION

In order to provide adequate performance, radio frequency (RF) circuits and systems require high quality inductors. Ideally, a high quality inductor has a large quality factor (Q), a sufficiently large inductance, relatively low resistance, and low capacitive coupling with the substrate. In addition, an ideal inductor does not have unwanted coupling with nearby circuit elements. Current silicon integrated circuit (IC) technologies, however, are unable to produce such ideal inductors due primarily to energy dissipation in the semiconductor substrate at high frequencies. Consequently, conventional RF circuits require off-chip inductors that add to the cost and power consumption of RF systems.

Extensive research has been carried out in attempt to develop techniques to integrate high quality IC inductors on silicon. Various geometric patterns for on-chip inductors have been considered. For example, a spiral inductor, a simple loop inductor, and a meander inductor are shown in FIGS. 1A, 1B, and 1C, respectively. Spiral inductors are considered to be the most feasible for silicon ICs since a given inductance can be attained using a spiral in less IC area than a loop or

a meander because of the significant positive mutual inductance existing in a spiral. Consequently, spiral inductors are the primary focus of research. For example, sophisticated techniques for designing optimal spiral IC inductors have been developed by C. Patrick Yue et al. in their article "A Physical Model for Planar Spiral Inductors on Silicon", International Electron Devices Meeting Technical Digest, December 1996. These general techniques can be used to design state of the art spiral inductors. Such inductors with an inductance of 2 nano-Henry (nH) have been integrated into silicon circuits using known fabrication technology. FIG. 2A shows such an inductor 10 together with four bands 12 representing magnetic field lines generated by the inductor. FIG. 2B shows a cut-away view of an IC 14 containing inductor 10. IC 14 has a silicon substrate 16, a conductive ground plane 18, and a silicon oxide layer 20. The quality factor (Q) of these inductors, however, is still limited to about 5 at 1 Giga-Hertz (GHz) and degrades to even smaller values at higher frequencies, due primarily to significant losses in the semiconducting silicon substrate. Self-resonance caused by parasitic capacitance between the inductor and the substrate also decreases the performance.

U.S. Pat. No. 5,539,241 to Abidi et al. discloses an approach to improve the performance of on-chip inductors. In order to reduce substrate coupling, a pit is etched under the inductor to create an empty insulating region between the inductor and the substrate. This approach, however, reduces the mechanical integrity of the inductor, and introduces unwanted cost and complexity to the fabrication process. Consequently, it is not considered a commercially viable solution.

In another attempt to improve IC inductor performance, R. Merrill et al. have proposed introducing a solid conducting ground shield between the inductor and the substrate in the article "Optimization of high Q integrated inductors in multi-level metal CMOS" presented at 1995 International

Electron Devices Meeting and at IEEE Electron Devices Society Santa Clara Valley Section 1996 Winter Half-Day Symposium. FIG. 3A shows such a solid ground shield together with magnetic field lines 24 generated by induced current 26 which is generated as explained below. Note that induced current is also equivalently referred to as image current, counter-current, or eddy current. FIG. 3B shows a cut-away view of an IC 28 containing a solid ground shield 22 positioned below inductor 10. The ground shield electrically isolates the inductor from the substrate and eliminates losses due to penetration of the inductor electric field into the substrate. Due to an induced image current in the ground shield, however, the effective inductance of the inductor is reduced by as much as 75%, and hence the Q is also significantly reduced. More specifically, currents flowing through the inductor 10 generate magnetic flux 12 as shown in FIGS. 2A and 3C. As high frequency currents change this flux, image currents 26 are induced in the shield 22 that oppose the change in flux, in accordance with Lenz's law. The magnetic field 24 due to the image current 26 opposes the magnetic field 12, thereby reducing the net magnetic field. As a result, this negative mutual coupling between the inductor current and the image current at high frequencies reduces the effective inductance and limits the inductor Q. Due to this substantial drawback, conventional ground shields are ineffective or counterproductive in attempts to improve inductor Q.

OBJECTS AND ADVANTAGES OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a technique for improving the performance of inductors in integrated circuits. In particular, it is an object of the invention to provide an integrated circuit inductor which can be fabricated using conventional integrated circuit techniques, which does not reduce the mechanical integrity of the IC, and which improves Q. It is a further object of the invention to provide a technique for electrically isolating on-chip inductors from the substrate

and from other electrical components on the chip without reducing the Q of the inductor. Other objects and advantages of the invention will become evident from the following description and accompanying figures.

SUMMARY OF THE INVENTION

The above objects and advantages are attained by a patterned ground shield positioned between the inductor and the substrate. In contrast with conventional solid ground shields, a ground shield in accordance with the present invention has a pattern of grounded conductive regions arranged to oppose the flow of an image current induced by the inductor. Preferably, the conductive regions are in the form of locally isolated conductive lines arranged substantially perpendicular to the conductive lines of the inductor, i.e. perpendicular to the image current that would be induced in a solid ground shield. As a result, the patterned ground shield effectively blocks the flow of undesired ground shield counter-currents, and hence prevents the undesired reduction of inductor magnetic field. At the same time, the ground shield blocks undesired penetration of the inductor electric field into the substrate and reduces both energy loss into the substrate and unwanted coupling between the inductor and other nearby circuit elements. Preferably, the spacing between adjacent conductive regions is minimized in order to provide optimal shielding between the inductor and the substrate, and the thickness of the ground shield is significantly smaller than the skin depth at the frequency of interest in order to minimize attenuation of the magnetic field. The ground shield may also be positioned above an inductor to provide a shield between the inductor and other circuit elements, such as capacitors or other inductors, which are fabricated above the inductor. For example, the shield may be positioned between two inductors that are used to form a transformer.

In one aspect of the invention, an integrated circuit is provided which comprises a substrate, a dielectric layer

which contacts the substrate at an interface, an inductor positioned above the substrate, usually fabricated in or on the dielectric layer, and a patterned ground shield fabricated below the inductor and above or near the interface of the substrate and the dielectric layer. The substrate may comprise a semiconductor material such as Si or GaAs, or a dielectric insulating material such as fused quartz or other glass. The dielectric layer may comprise one or more layers of dielectric materials such as SiO_2, low-κ polymer (i.e., a polymer whose dielectric constant κ is lower than that of SiO_2), or air. The patterned ground shield is composed of a conductor, such as polysilicon, aluminum, or copper, and the inductor is composed of a conductor such as aluminum or copper. The ground shield comprises a plurality of grounded conductive regions arranged in a geometrical pattern that serves to substantially inhibit the induction of image current in the ground shield by the current in the inductor. The patterned ground shield is preferably fabricated in the dielectric layer, at or above the interface, or possibly in the substrate itself, near the interface. The conductive regions of the ground shield are mutually grounded, but locally isolated from each other by insulating slots. In the preferred embodiment, the conductive regions are conductive line segments oriented perpendicular to the conductive lines of the inductor just above them. In the case of a rectangular or square spiral inductor, these conductive lines form a comb pattern on each of four edges of the ground shield.

DESCRIPTION OF THE FIGURES

FIG. **1A** is a schematic of a conventional spiral inductor.

FIG. **1B** is a schematic of a conventional loop inductor.

FIG. **1C** is a schematic of a conventional meander inductor.

FIG. **2A** is a perspective view of a conventional spiral inductor with its associated magnetic field lines.

FIG. **2B** is a cut-away view of a conventional spiral inductor as fabricated in a silicon integrated circuit.

FIG. **3A** is a perspective view of a conventional solid ground shield showing the induced image current and associated magnetic field lines.

FIG. **3B** is a cut-away view of a spiral inductor and solid ground shield as fabricated in a conventional silicon integrated circuit.

FIG. **3C** is a cross-sectional view of a conventional spiral inductor and its associated magnetic field.

FIG. **4A** is a cut-away view of a spiral inductor and patterned ground shield as fabricated in the silicon oxide layer of a silicon integrated circuit in accordance with the present invention.

FIG. **4B** is a cut-away view of a spiral inductor and patterned ground shield as fabricated in the silicon substrate of a silicon integrated circuit in accordance with the present invention.

FIG. **4C** is a perspective view of a patterned ground shield according to the present invention.

FIG. **4D** is a top view of a rectangular spiral inductor and patterned ground shield according to a preferred embodiment of the present invention, indicating the orthogonal relationship of their respective conductive lines.

FIG. **4E** is a top view of a spiral inductor and patterned ground shield according to an alternate embodiment of the present invention, wherein the inductor and ground shield have octagonal shapes.

FIG. **4F** is a top view of a patterned ground shield designed for use with a spiral inductor having a square shape, in accordance with the present invention.

FIG. **4G** is a top view of a patterned ground shield designed for use with a spiral inductor having a circular shape, in accordance with the present invention.

FIG. **4H** is a top view of a patterned ground shield having a very simple pattern, in accordance with the present invention.

FIG. **4I** is a top view of a patterned ground shield having a relatively complex pattern, in accordance with the present invention.

FIG. **4J** is a top view of a patterned ground shield having a pattern of many parallel conductive lines, in accordance with the present invention.

FIG. **4K** is a top view of a patterned ground shield having a pattern of parallel conductive lines, in accordance with the present invention.

FIG. **5A** is a graph of inductor Q with respect to frequency for a patterned aluminum ground shield, a solid aluminum ground shield, and two cases of no ground shield.

FIG. **5B** is a graph of inductor Q with respect to frequency for a patterned polysilicon ground shield, a solid polysilicon ground shield, and two cases of no ground shield.

FIG. **5C** is a graph of substrate coupling between adjacent inductors with respect to frequency for a patterned polysilicon ground shield, and two cases of no ground shield.

FIG. **6A** is a top view of two adjacent inductors whose coupling is indicated in FIG. 5C.

FIG. **6B** is a top view of a patterned polysilicon ground shield positioned beneath each of the inductors shown in FIG. 6A.

FIG. **7** is a perspective view of a patterned ground shield positioned between two inductors in accordance with the present invention.

DETAILED DESCRIPTION

Although the following detailed description contains many specifics for the purposes of illustration, anyone of ordinary skill in the art will appreciate that many variations and alterations to the following details are within the scope of the invention. Accordingly, the following preferred embodiment of the invention is set forth without any loss of generality to, and without imposing limitations upon, the invention.

In accordance with a preferred embodiment of the invention, a patterned ground shield 30 is fabricated in the silicon oxide layer 20 of an IC 32 directly below a spiral inductor 10 as shown in FIG. 4A. Alternatively, as shown in FIG. 4B, patterned ground shield 30 is fabricated in the silicon substrate layer near its interface with the silicon oxide layer. In contrast to a conventional solid ground shield, as shown in FIG. 3A, the patterned ground shield 30 of the present invention is a grating composed of a collection of locally isolated conductive lines 34 locally separated by slots 35, as shown in FIG. 4C. Although the conductive lines 34 are locally isolated, they are mutually grounded. For optimal obstruction of the image current, each of the conductive lines 34 in the ground shield grating 30 is positioned orthogonal to the conductive line segments in the inductor 10 directly above it, as shown in FIG. 4D. Because these conductive lines are perpendicular to the inductor's conductive lines, the patterned ground shield 30 does not permit the flow of counter-currents induced by changes in the flux through the inductor. Therefore, the performance of inductor is not reduced by these induced counter-currents, as is the case with a conventional ground shield. The slots 35, which separate adjacent conductive lines of the ground shield, are preferably very narrow in comparison with the width of the conductive lines. As a result, the patterned ground shield still blocks the penetration of electric field of the inductor into the substrate. Accordingly, the performance of the inductor is not reduced by losses arising from penetration of the electric field into the substrate, and coupling through the substrate between the inductor and other nearby circuit elements is reduced. Preferably, the thickness of the ground shield is significantly less than the skin depth at the frequency of interest in order to avoid attenuation of the magnetic field and reductions of the effective inductance of the inductor.

Those skilled in the art will appreciate that the principles of the present invention are not limited to the rectilinear spiral inductors used in the preferred embodiment, but applies generally to spiral inductors of any geometrical arrangement, such as hexagonal, pentagonal, octagonal, and curved spiral inductors. For example, FIG. 4E illustrates an octagonal inductor 36 and a corresponding patterned ground shield underneath the inductor. The conductive lines 34 of the ground shield are oriented roughly perpendicular to the conductive lines of the inductor. Generally, the conductive lines in a patterned ground shield are optimally arranged when they are oriented perpendicular to the conductive lines in the inductor. For example, FIG. 4F shows a patterned ground shield optimized for a spiral inductor having the shape of a square, while FIG. 4G illustrates a patterned ground shield optimized for a spiral inductor having the shape of a circle, or a polygon having many sides. Although it is normally preferable to pattern the ground shield so that all the conductive lines are oriented perpendicular to the lines of the inductor, significant reduction in ground shield image current can also be obtained with other patterns. For example, FIGS. 4H and 4I show two ground shields with patterns of parallel conductive lines. Patterns of this type are not optimal for spiral inductors since they contain conductive lines oriented parallel to the conductive lines of the inductor. Nevertheless, because these patterns still inhibit the flow of the image current, they are far superior to solid ground shields. Note also that these patterns can be very effective in conjunction with a meander inductor (FIG. 1C). Very simple patterns, such as that shown in FIG. 4J, can also be effective with spiral inductors, even though they are not optimal. Very complex fractal-like patterns, such as shown in FIG. 4K, are also effective.

The patterns shown in FIGS. 4J and 4K do not have conductive lines with well-defined orientation. Rather, they have locally isolated conductive regions defined by the slots which separate them. The slots, however, have well-defined

orientations. As a result, the effective orientation of the conductive regions corresponds to the orientation of these slots. Accordingly, for the purposes of this description, the orientation of the conductive lines or regions is considered to be equivalent to the average orientation of the slots which define them.

The slots 35 between the conductive lines 34 act as an open circuit to cut off the path of the induced loop current. The slots should be sufficiently narrow such that the vertical electric field cannot leak through the patterned ground shield 30 into the underlying silicon substrate. With the slots 35 etched away, the conductive lines 34 serve as the termination for the electric field generated by the inductor. The conductive lines are connected together around outer edges forming a perimeter of the ground shield. In order to inhibit unwanted loop current around this perimeter, the ground shield of the preferred embodiment contains a slot 37 in the perimeter. FIG. 4J also illustrates the use of more than one slot 37 to prevent a current around the perimeter of the ground shield. In addition, the shield should be provided with a low-impedance connection to ground. The general design goal is to prevent negative mutual coupling while minimizing the impedance to ground.

Those skilled in the art will also appreciate that the patterned ground shield need not be connected to DC ground, but will provide the same shielding effect if it is connected to a potential that is relatively low in frequency in comparison to the inductor AC frequency. Accordingly, the term "ground shield" in the context of the present invention is not limited to a DC ground shield.

A cut-away of a portion of an integrated circuit 32 made in accordance with the present invention is shown in FIG. 4A. The integrated circuit 32 comprises an inductor 10 and patterned ground shield 30 fabricated on a 10 to 20 Ω-cm silicon substrate 16 using photolithography techniques well

known in the art of silicon IC manufacturing. Although a silicon substrate is preferred, those skilled in the art will appreciate that the principles of the present invention are independent of the specific materials used. In particular, gallium arsenide and other substrates may also be used to fabricate ICs containing patterned ground shields. The typical thickness of the silicon substrate is on the order of 300 to 1200 microns, depending on the silicon wafer diameter. The oxide layer containing the inductor and ground shield is typically about 5 to 10 microns thick.

In a typical silicon IC making use of the present invention, a conductive metal ground plane 18, which is part of the IC package, is attached beneath the silicon substrate 16. Due to the relatively large thickness of the silicon substrate 16, however, the ground plane 18 beneath the substrate has virtually no influence on the behavior of the inductor and the effectiveness of the patterned ground shield. Thus, the presence, absence, or properties of the ground plane 18 is irrelevant to the problem that is addressed by the invention.

Conventional photolithography techniques are used to fabricate on top of the silicon substrate 16 a patterned ground shield 30 and an 8 nH inductor 10 within a layer of silicon oxide 20. FIG. 4C is a perspective view of a ground shield 30 according to the present invention. The ground shield is approximately 300 microns wide, with slots 35 and 37 having widths on the order of 1 to 2 microns, and conductive lines 34 having widths on the order of 5 to 20 microns. In the preferred embodiment, the ground shield 30 is positioned between the inductor 10 and the silicon substrate 16, as shown in FIG 4A. The ground shield 30 is composed of 0.5 micron thick 12 Ω/sq. polysilicon or other suitable conductive material, and the inductor 10 is composed of a 2 micron thick 12 mΩ/sq. aluminum alloy or other appropriate conductive material. The oxide thickness between the ground shield and the inductor is about 6 microns, and the ground shield is separated from the substrate by 0.4 microns of

oxide. The resistance of the ground shield is an important design parameter. The purpose of the patterned ground shield is to provide the electric field with a good short to ground. Since a finite shield resistance contributes to the energy loss of the inductor, it should be kept minimal. Specifically, by keeping the shield resistance small compared to the reactance of the oxide capacitance, the voltage drop that can develop across the shield resistance is very small. As a result, the energy loss due to the shield resistance is insignificant compared to other loses. A typical on-chip spiral inductor has parasitic oxide capacitance between 0.25 to 1.0 pico-Farad (pF) depending on the inductor size and the oxide thickness. The corresponding reactance due to the oxide capacitance at 1 to 2 GHz is on the order of 100 Ω, and hence a shield resistance of a few Ohms is sufficiently small not to cause any noticeable loss.

Those skilled in the art will appreciate that inductors used with patterned ground shields according to the present invention may be optimized using general purpose techniques known in the art, such as those taught by C. Patrick Yue et al. in the article reference above.

The improvement in inductor Q attained by the techniques of the present invention is shown in FIGS. 5A and 5B. In FIG. 5A the inductor Q is graphed with respect to frequency for four cases: an inductor with no ground shield and an 11 Ω-cm silicon substrate (NGS 11), an inductor with no ground shield and a 19 Ω-cm silicon substrate (NGS 19), an inductor with a solid 64 mΩ/sq. aluminum ground shield (Al-SGS), and an inductor with a patterned 64 mΩ/sq. aluminum ground shield (Al-PGS). The solid ground shield Q is significantly reduced because of the relatively high conductivity of aluminum. The high conductivity allows large currents to be induced that oppose the magnetic flux created by the inductor and reduce its inductance.

In FIG. 5B the inductor Q is also graphed for four cases: an inductor with no ground shield and an 11 Ω-cm silicon substrate (NGS 11), an inductor with no ground shield and a 19 Ω-cm silicon substrate (NGS 19), an inductor with a solid 12 Ω/sq. polysilicon ground shield (Poly-SGS), and an inductor with a patterned 12 Ω/sq. polysilicon ground shield (Poly-PGS). The improvement in the inductor Q due to the patterned ground shield is evident in both FIG. 5A and FIG. 5B. In particular, the polysilicon patterned ground shield yields up to 33% improvement in Q at 1 to 2 GHz.

The present invention also reduces substrate coupling between adjacent circuit elements by shielding the inductors from the substrate. For example, FIG. 6A illustrates two adjacent inductors 10, each positioned above a patterned ground shield 30, such as shown in FIG. 6B. The modulus of the transmission coefficient, i.e. $|S_{12}|$, can be used to measure the substrate coupling between the inductors. FIG. 5C shows a graph of the coupling with respect to frequency for three cases: with no ground shield and an 11 Ω-cm silicon substrate (NGS 11), with no ground shield and a 19 Ω-cm silicon substrate (NGS 19), and with a 12 Ω/sq. polysilicon patterned ground shield (Poly-PGS). It is evident from the figure that the substrate coupling is significantly reduced by the patterned ground shield. In particular, inductors with polysilicon patterned ground shields show improved isolation up to 25 dB at GHz frequencies.

The use of a patterned ground shield has many benefits in addition to those previously mentioned. For example, because the inductor is isolated from the substrate, inductor behavior is independent of variations in substrate resistivity and type. Consequently, the inductor behavior is easier to model, especially at different temperatures. Moreover, the large silicon area under the inductor potentially can be used for device fabrication. Also, the patterned ground shield can be incorporated easily into present IC fabrication with no additional process steps.

In another aspect of the invention, a patterned ground shield is positioned above an inductor to provide a shield between the inductor and other circuit elements, such as capacitors or other inductors, which are fabricated above the inductor. The patterned ground shield allows these other circuit elements to be placed in close physical proximity to the underlying inductor without unwanted electrical coupling with the inductor. This aspect of the invention allows space above the inductor to be used for other circuitry, thereby making more efficient use of chip area. In one example of this use of the patterned ground shield, the shield 30 is positioned between two spiral inductors 10, as shown in FIG. 7, to form an on-chip transformer. Because the patterned ground shield filters the high frequency electric fields, but allows the high frequency magnetic fields to pass, the two inductors are magnetically coupled without unwanted electrical coupling.

It will be appreciated that the dielectric layer may be a single material, such as silicon oxide, or a composite layer comprising multiple layers of different dielectric materials. For example, the dielectric layer may comprise a low-κ layer on top of an oxide layer. In the case of flip-chip fabrication, the dielectric layer may comprise a layer of air between the chips, as well as one or more layers of oxide.

In silicon IC technology, the fabrication process varies substantially between chips, resulting in a variation in many specific dimensions and design parameters. These and other variations and applications of the principle of the present invention are therefore considered to be within the spirit and scope of the present invention. Accordingly, the present invention should not be construed to be limited to the specific examples shown, but by the following claims and their legal equivalents.

Claims

1. An integrated circuit comprising:
a substrate;
a dielectric layer contacting the substrate at an interface;
an inductor fabricated above the substrate, wherein the inductor comprises conductive lines; and
a patterned ground shield fabricated below the inductor and above or near the interface;
wherein the ground shield comprises a plurality of grounded conductive regions arranged in a geometrical pattern substantially inhibiting an inducement of an image current in the ground shield by a current in the inductor.

2. The integrated circuit of claim 1 wherein the conductive lines of the inductor are arranged in the form of a spiral.

3. The integrated circuit of claim 1 wherein the patterned ground shield is fabricated above the substrate.

4. The integrated circuit of claim 1 wherein the patterned ground shield is fabricated in the substrate.

5. The integrated circuit of claim 1 wherein the conductive regions of the ground shield are mutually grounded but locally isolated from each other.

6. The integrated circuit of claim 1 wherein the grounded conductive regions comprise conductive line segments oriented perpendicular to the conductive lines of the inductor.

7. The integrated circuit of claim 1 wherein the grounded conductive regions comprise a comb pattern of conductive line segments.

8. The integrated circuit of claim 1 wherein the substrate comprises a semiconductor material chosen from the group consisting of GaAs and silicon.

9. The integrated circuit of claim 1 wherein the substrate comprises a dielectric material.

10. The integrated circuit of claim 1 wherein the dielectric layer comprises silicon oxide.

11. The integrated circuit of claim 1 wherein the dielectric layer comprises a polymer.

12. The integrated circuit of claim 1 wherein the conductive regions of the ground shield are composed of polysilicon.

13. The integrated circuit of claim 1 wherein the conductive regions of the ground shield are composed of aluminum.

14. The integrated circuit of claim 1 wherein the conductive regions of the ground shield are composed of copper.

15. The integrated circuit of claim 1 wherein the conductive lines of the inductor are composed of aluminum.

16. The integrated circuit of claim 1 wherein the conductive lines of the inductor are composed of copper.

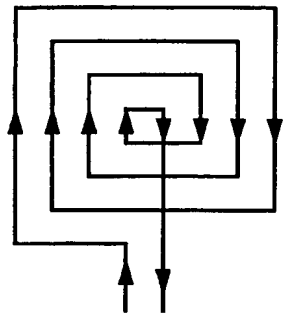


FIG. 1A
(PRIOR ART)

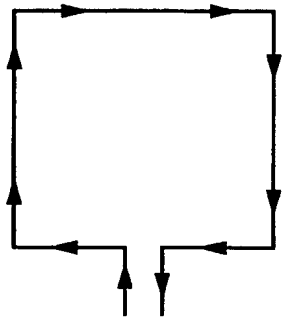


FIG. 1B
(PRIOR ART)

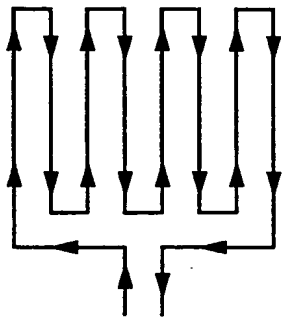


FIG. 1C
(PRIOR ART)

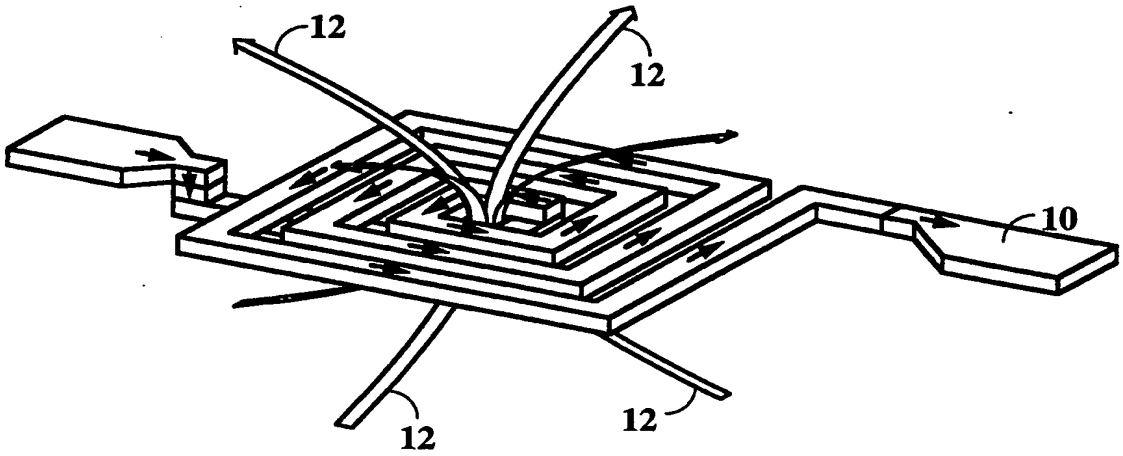


FIG. 2A
(PRIOR ART)

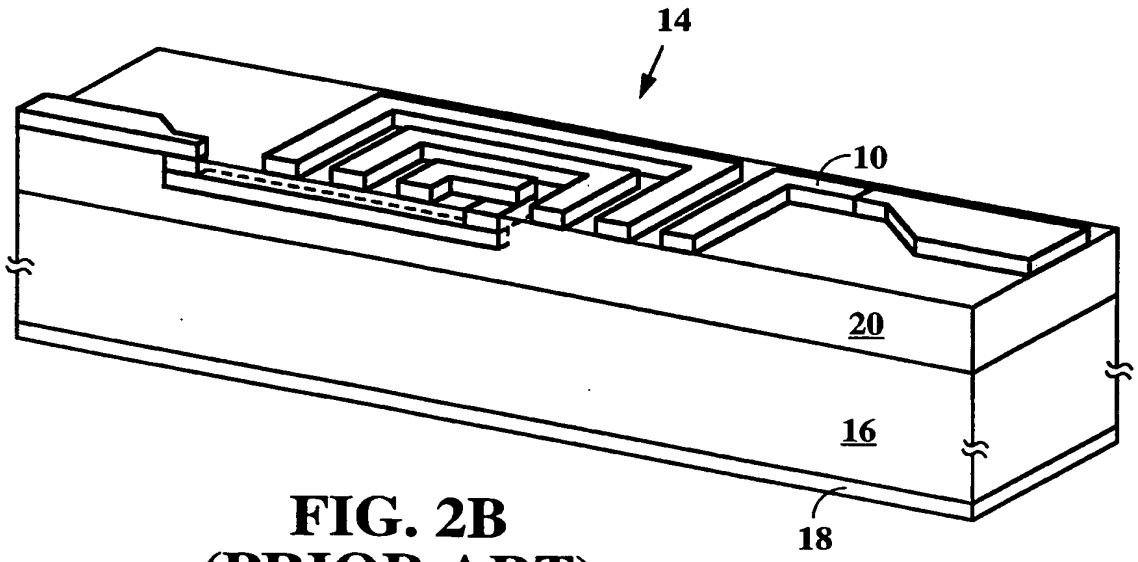


FIG. 2B
(PRIOR ART)

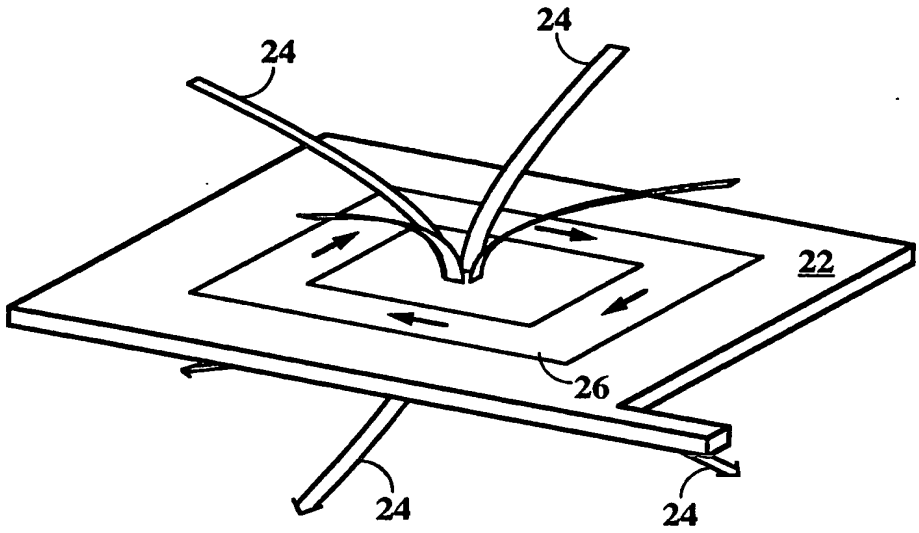


FIG. 3A
(PRIOR ART)

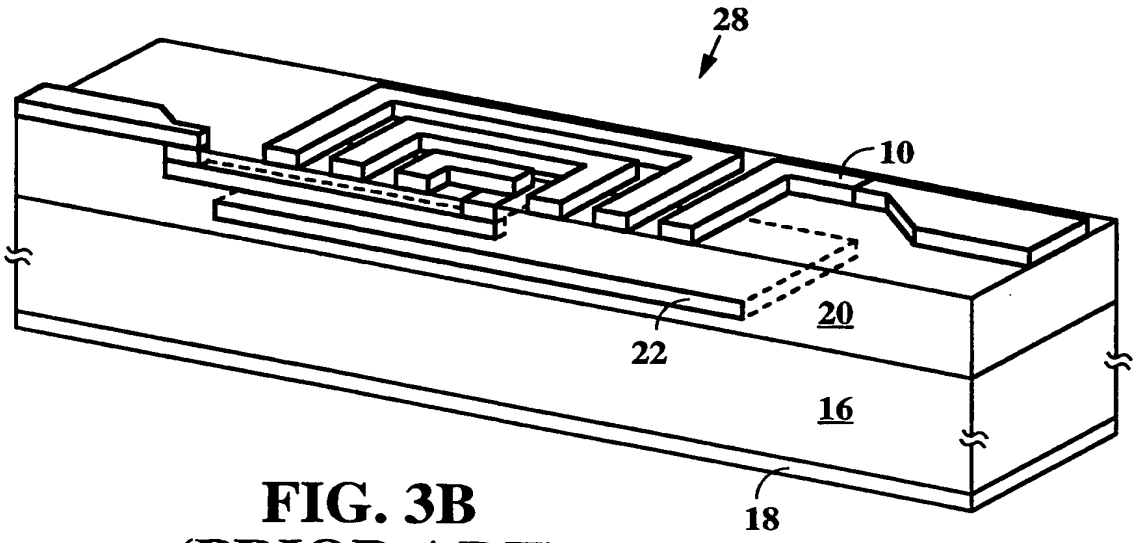


FIG. 3B
(PRIOR ART)

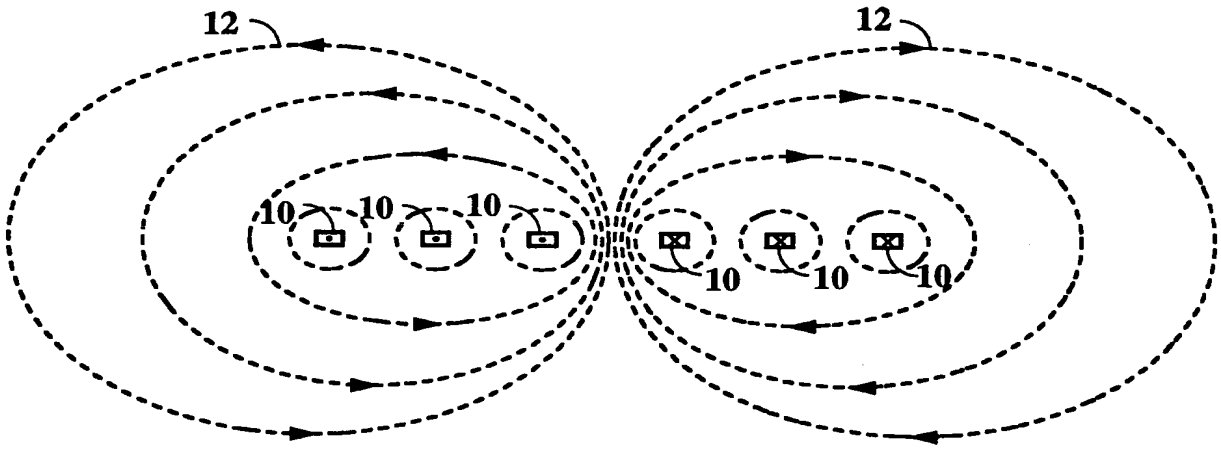


FIG. 3C
(PRIOR ART)

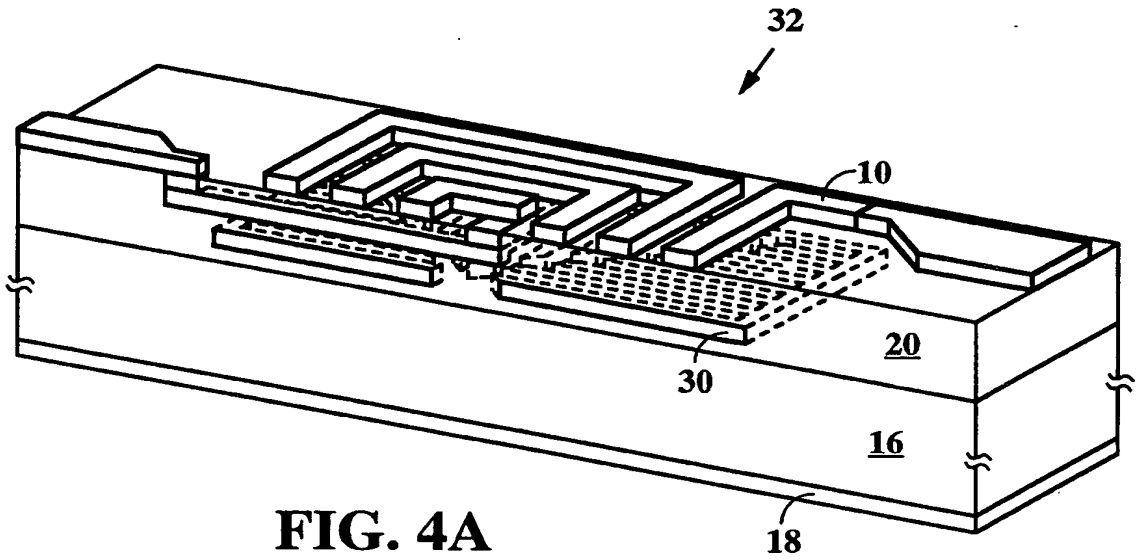


FIG. 4A

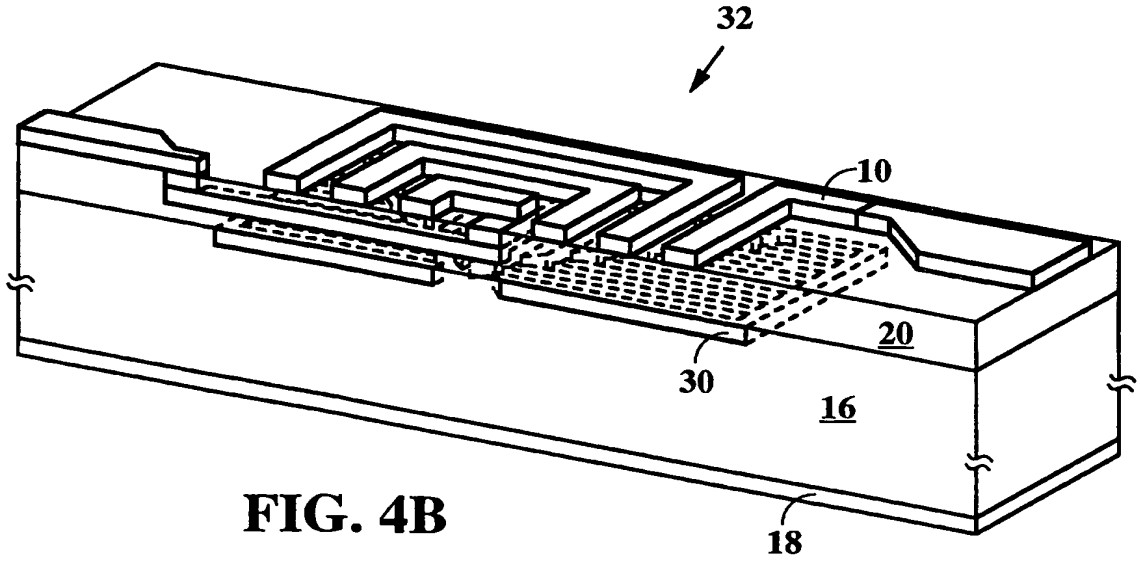


FIG. 4B

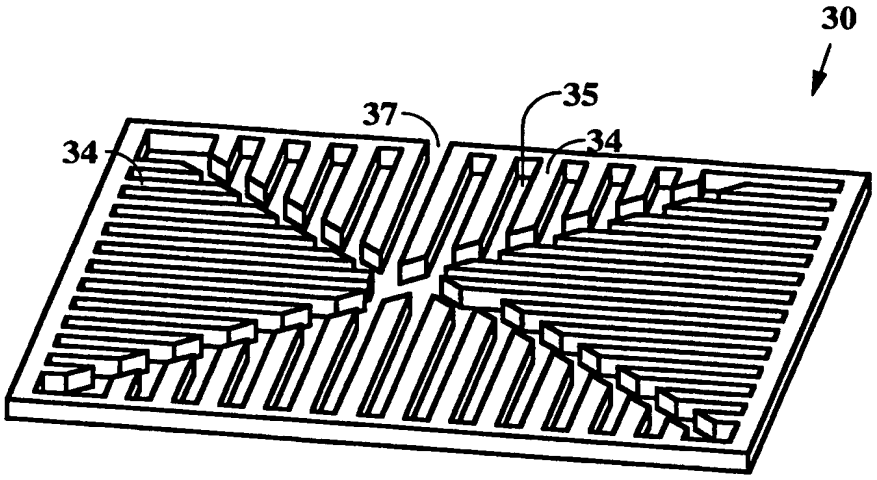


FIG. 4C

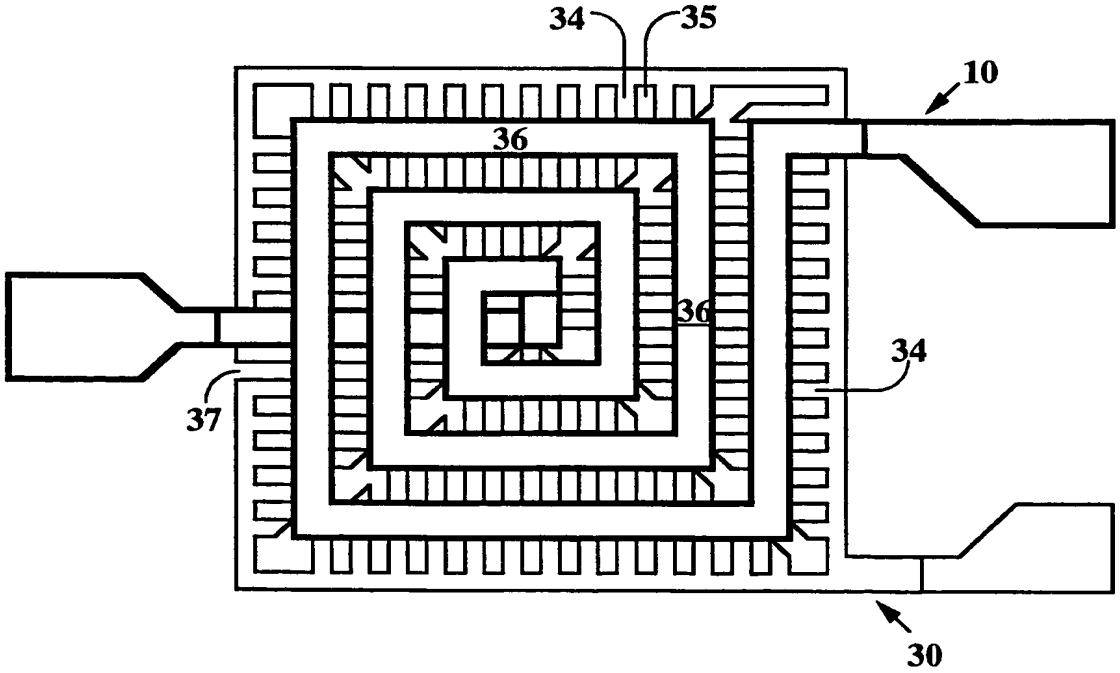


FIG. 4D

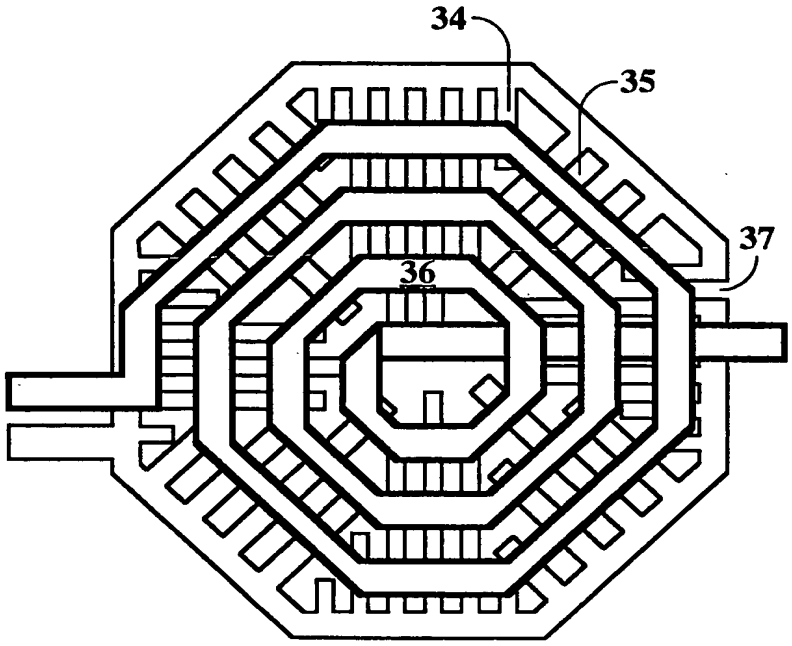


FIG. 4E

FIG. 4F

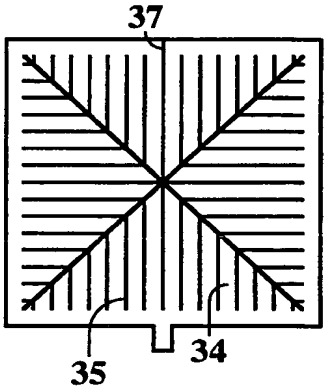


FIG. 4G

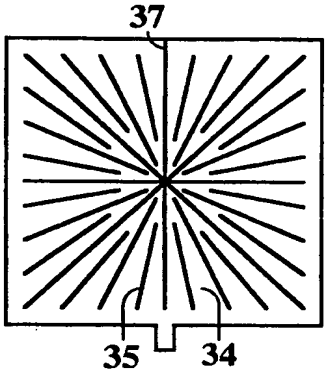


FIG. 4H

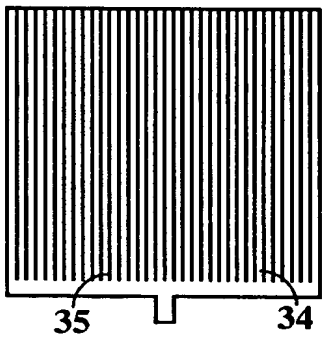


FIG. 4I

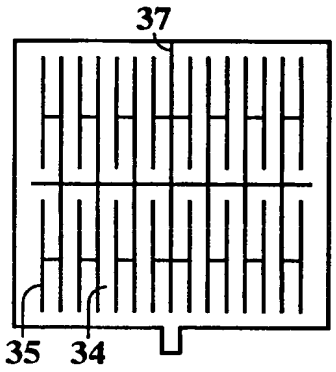


FIG. 4J

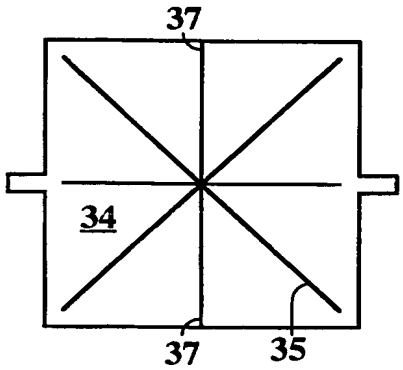
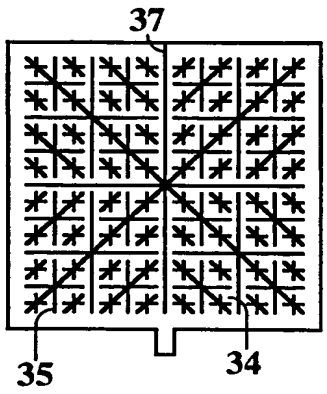


FIG. 4K



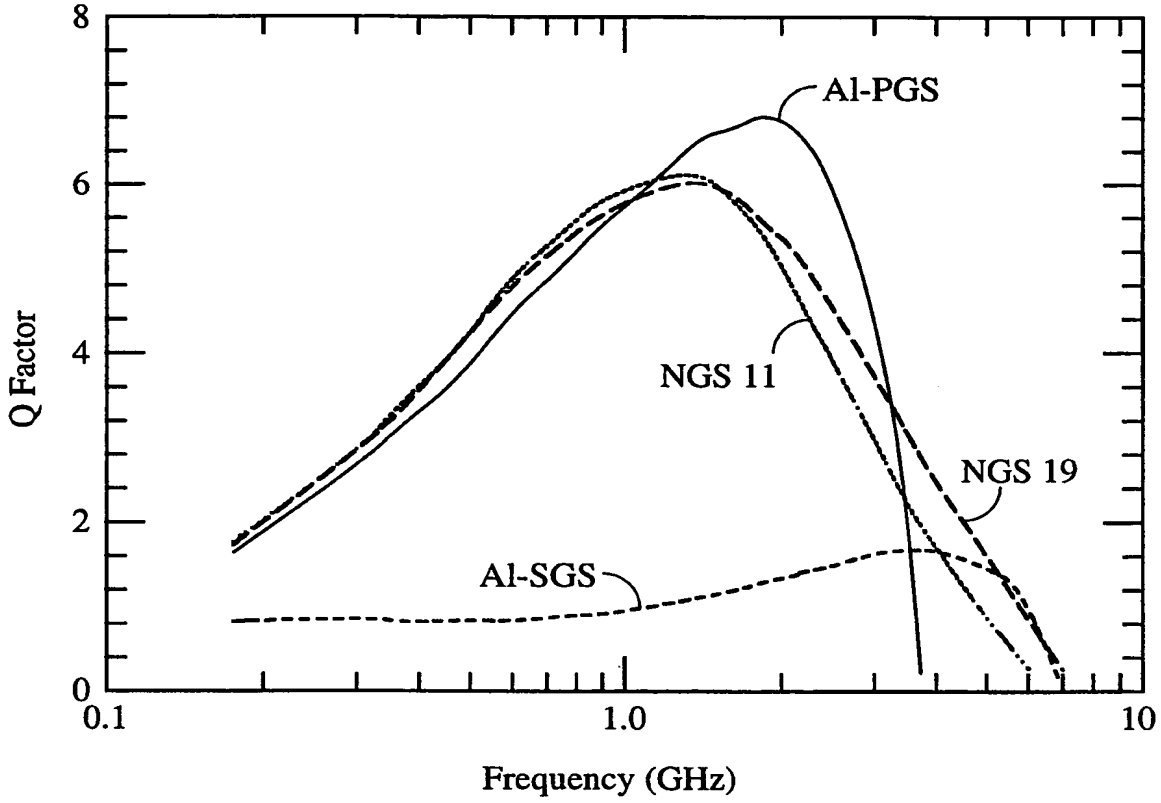

8
6
4
2
0
Q Factor
0.1
1.0
10
Frequency (GHz)
Al-PGS
NGS 11
NGS 19
Al-SGS

FIG. 5A

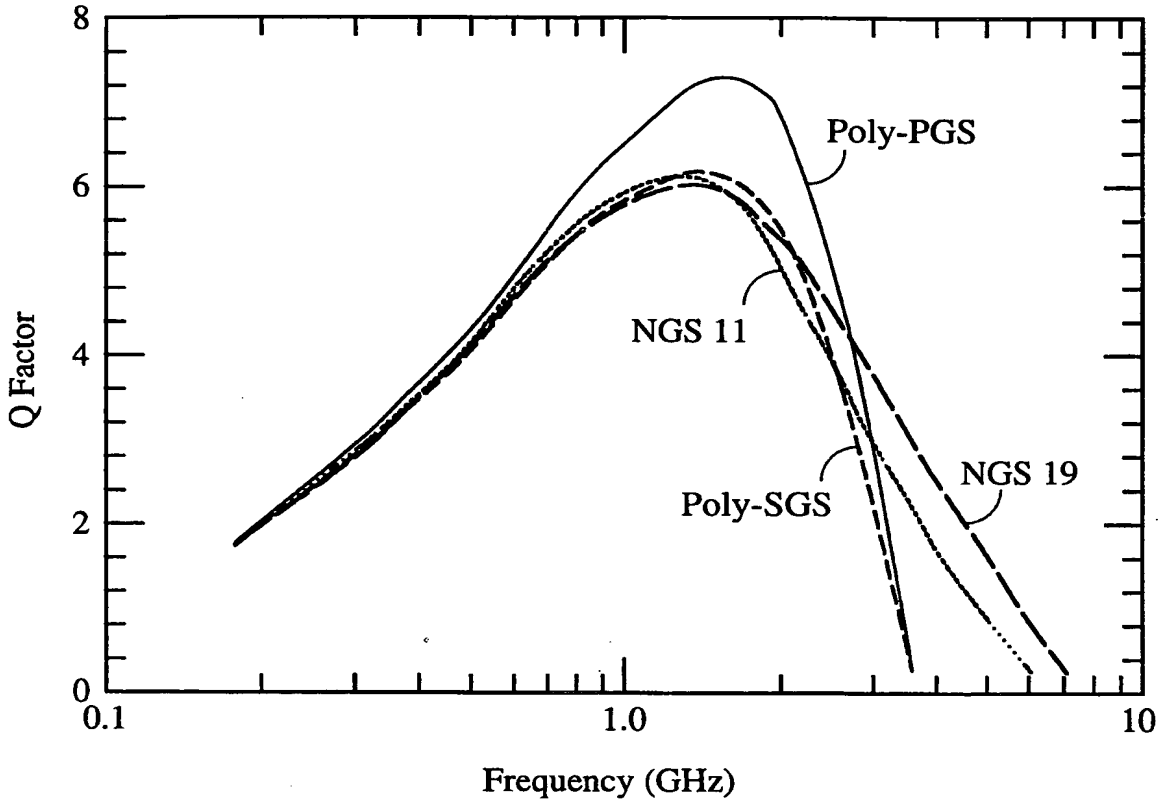

8
6
4
2
0
Q Factor
0.1
1.0
10
Frequency (GHz)
Poly-PGS
NGS 11
NGS 19
Poly-SGS

FIG. 5B

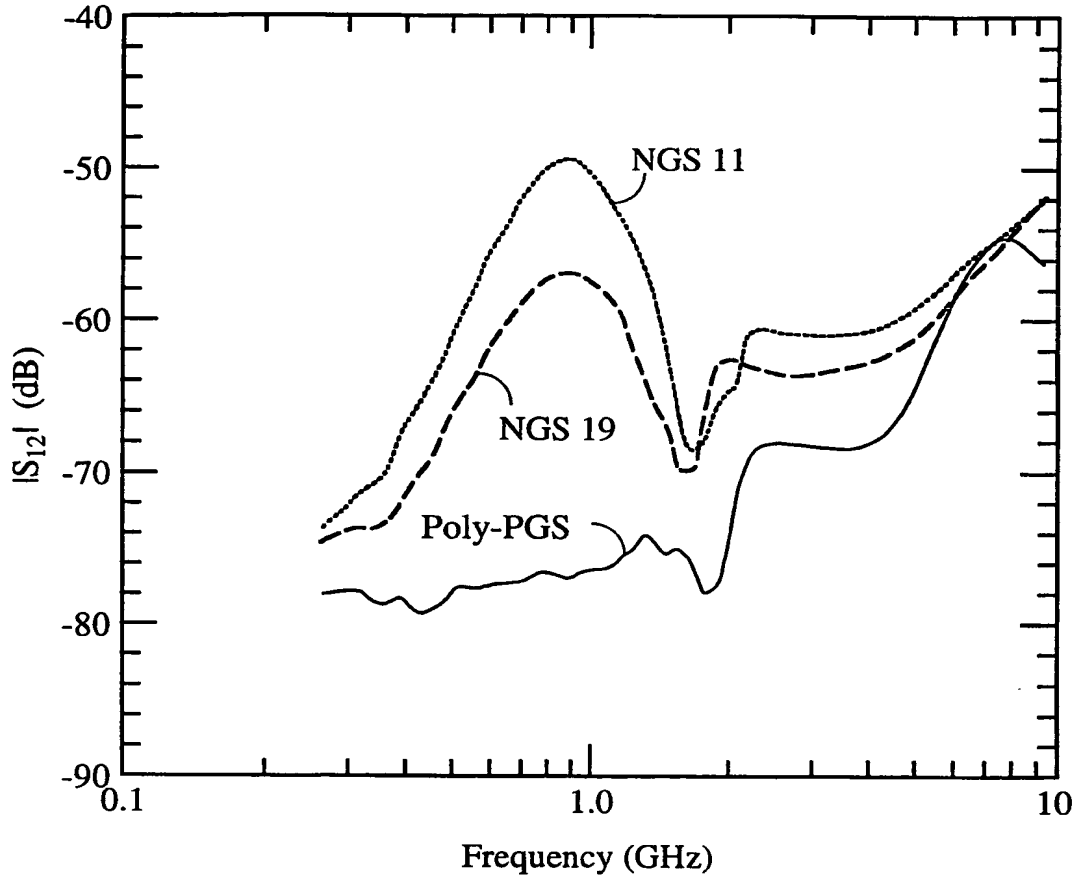

-40
-50
-60
-70
-80
-90
$|S_{12}|$ (dB)
NGS 11
NGS 19
Poly-PGS
0.1
1.0
10
Frequency (GHz)

FIG. 5C

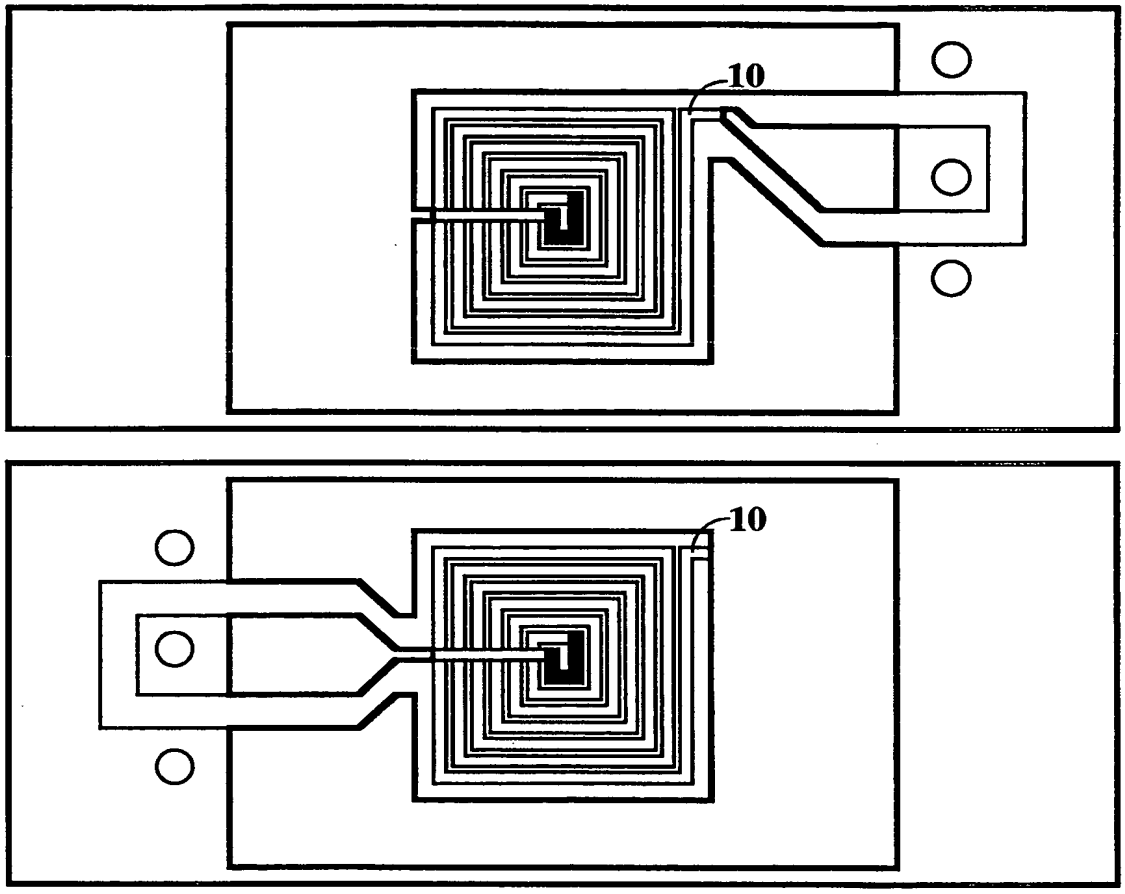


FIG. 6A

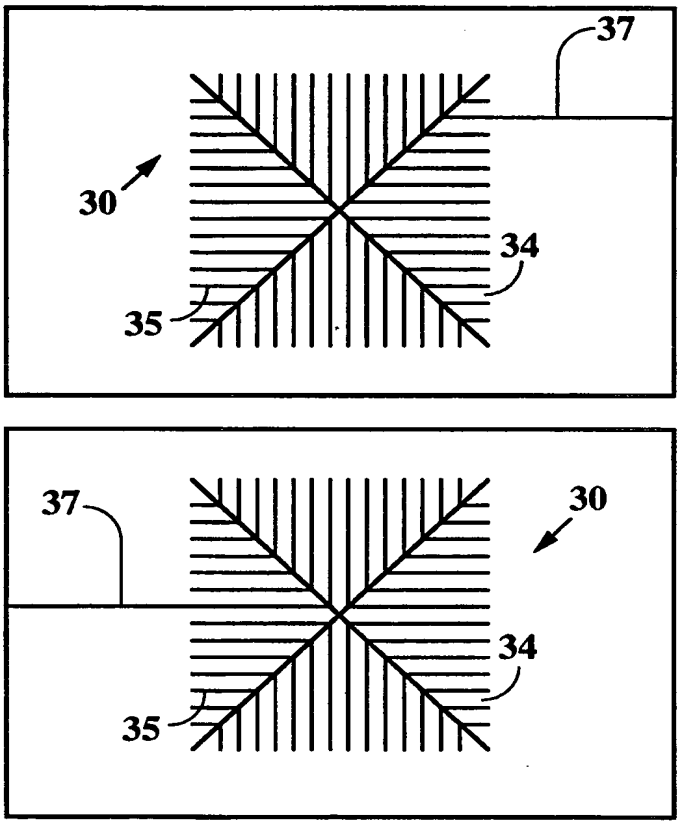


FIG. 6B

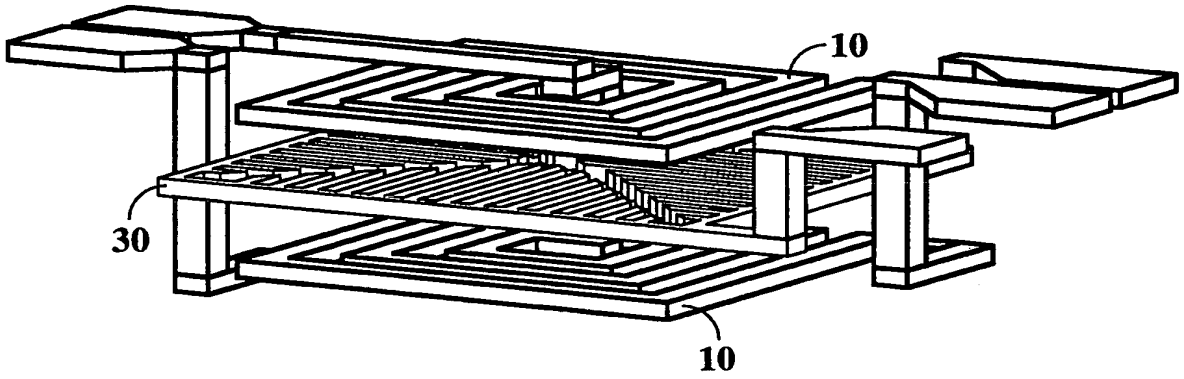


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/05149

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 29/00
US CL :257/531, 508

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/531, 508, 379, 659, 758

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,541,442 A (KEIL ET AL) 30 July 1996 (30/07/96), see entire document.	1-16
A	US 5,483,207 A (GABARA) 09 January 1996 (09/01/96), see entire document.	1-16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
21 MAY 1998

Date of mailing of the international search report
22 JUL 1998

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Form PCT/ISA/210 (second sheet)(July 1992)*